IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellent:	Pan et al.	Docket No.:	TI-31192
Serial No.:	09/998,606	Examiner:	Nguyen, C.
Filed:	11/30/01	Art Unit:	2811
Customer No.:	23494	Conf. No.:	4902
For:	HIGH DENSITY CAPACITOR USING TOPOGRAPHIC SURFACE		

CORRECTED APPEAL BRIEF

August 1, 2008

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is Appellant's Appeal Brief filed pursuant to 37 C.F.R. §1.192 and the Notice of Appeal filed 2/11/2008.

Real Party in Interest under 37 C.F.R. §1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. §1.192(c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of the Claims on Appeal under 37 C.F.R. §1.192(c)(3)

Claims 18-22 are pending in this case.

Claims 1-17 are cancelled.

Claims 18-22 are appealed.

Status of Amendments Filed After Final Rejection under 37 C.F.R. §1.192(c)(4)

No amendments were filed after final rejection.

Summary of Claimed Subject Matter

The invention of claim 18 is an integrated circuit having an analog circuit stage. The integrated circuit comprises a semiconductor layer having a plurality of recesses formed therein as shown in FIG. 3a, 5a. A dielectric layer (e.g., 304, FOX) is formed over the semiconductor layer including within the recesses as shown in Fig. 3b, 5b. A parallel plate capacitor (306-310) is formed over the dielectric layer as shown in FIG. 3c, 5c. The parallel plate capacitor extends into and out of the recesses in the semiconductor layer. (See, specification page 6 lines 5-19 and page 9 lines 7-24) This provides the advantage of increased capacitor surface area which reduces the overall required die size by as much as 5-12% without requiring new mask levels as described on page 7 lines 5-11.

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 18-20 were properly rejected under 35 U.S.C. § 103 as being unpatentable over Vaartstra in view of Ouellet et al.

2. Whether claims 21-22 were properly rejected under U.S.C. § 103 as being unpatentable over Vaartstra in view of Ouellet et al and Maniar.

Statement of the Grouping of Claims under 37 C.F.R. §1.192(c)(7)

Claims 18-20 stand or fall together.

Claims 21-22 stand or fall together.

Arguments

Whether claims 18-22 were properly rejected under 35 U.S.C. § 103 as being unpatentable over Vaartstra in view of Ouellet et al.

Appellant respectfully submits that the Examiner improperly rejected claim 18 as unpatentable over Vaartstra in view of Ouellet et al. In order to form a *prima facie* case of obviousness, the cited references must teach or suggest all the claim limitations. The combination of Vaartstra and Ouellet fails to teach or suggest all the claim limitations. Specifically, there is no disclosure or suggestion in the references of a parallel plate capacitor that extends into and out of recesses in the semiconductor layer.

The Examiner in fact notes, on page 2 of the Office Action, that "Vaartstra does not teach . . . the parallel plate capacitor extending into and out of plurality of recesses in the semiconductor layer." However, the Examiner goes on to argue (page 3) that Vaartsta's Fig. 1 is not drawn to scale and so "the parallel plate capacitor actually may be extending into and out of plurality of recesses in the semiconductor layer." Fig. 1 of Vaartstra shows a memory cell in which a ferroelectric material 11 is formed between two electrodes 12 and 13. The bottom electrode 13 is formed on layer 14 (e.g., silicon dioxide). While the underlying layer 14 extends into the topology of the substrate, as shown in FIG. 1, layer 14 fills this substrate topology and no part of the memory cell extends into or out of recesses in the substrate. Not only does a capacitor not extend into and out of recesses in a semiconductor layer, but no part of the capacitor extends into and out of a recess in the semiconductor layer. The topology shown in FIG. 1 is not

mentioned in the text of the patent. There is no discussion as to its purpose or depth. There is nothing in Vaartstra to suggest a recess other than the topology illustrated in Fig. 1. There is certainly no suggestion of modifying a depth of the recess such that a parallel plate capacitor extends into and out of recesses in a semiconductor layer.

The Examiner further argues that depth of recesses is considered as "an art recognized variable of importance which is subject to routine experimentation and optimization." If Vaartstra taught a parallel plate capacitor extending into and out of recesses in a semiconductor layer, the depth of those recesses may be considered routine experimentation. However, Vaartstra teaches a memory cell over a substrate. While the substrate is illustrated with topology, the topology is not discussed in the text. There is no disclosure or suggestion of the general concept of a parallel plate capacitor extending into and out of recesses in a semiconductor layer. This novel concept is more than a mere optimization. It is not taught or suggested by the prior art.

The Examiner also argues on page 3 that it "would have been obvious to one of ordinary skill in the art to the recess deep enough so that the parallel plate capacitor extending into and out of plurality of recesses in the semiconductor layer *in order to increase the effective area of the capacitor structure* . . . ." (emphasis added) However, the prior art fails to teach any reason for the topology shown in Fig. 1, much less the rationale supplied by the Examiner of increasing the effective area of the capacitor structure. The advantage of increasing the effective area of the capacitor structure is provided by the instant application and not by Vaartstra in combination with the other references. The Examiner is improperly using hindsight (gained from the instant application) to reject the claims.

Vaartstra teaches a memory cell rather than a parallel plate capacitor of an analog circuit stage as claimed. Ouellet is applied to teach a capacitor structure for a memory device or analog circuit stage. Ouellet is not applied to teach or suggest a

parallel plate capacitor that extends into and out of recesses in the semiconductor layer and, as discussed above, Vaartstra does not teach a parallel plate capacitor that extends into and out of recesses in the semiconductor layer. Accordingly, the combination of Ouellet and Vaartstra fails to disclose or suggest a parallel plate capacitor that extends into and out of recesses in the semiconductor layer. Since the combination of Vaartstra and Ouellet fails to teach or suggest all the claim elements, the Examiner has not established a *prima facie* case of obviousness and thus, claim 18 and the claims dependent thereon were improperly rejected.

Whether claims 21-22 were properly rejected under U.S.C. § 103 as being unpatentable over Vaartstra in view of Ouellet et al and Maniar.

Appellant respectfully submits that the Examiner improperly rejected claims 21-22 as unpatentable over Vaartstra in view of Ouellet et al and Maniar. In order to form a *prima facie* case of obviousness, the cited references must teach or suggest all the claim limitations. The combination of Vaartstra, Ouellet and Maniar fails to teach or suggest all the claim limitations. Specifically, there is no disclosure or suggestion in the combined references of a parallel plate capacitor that extends into and out of recesses in the semiconductor layer, as required by claim 18 from which claims 21 and 22 depend.

As discussed above the combination of Vaartstra and Ouellet fails to disclose or suggest a parallel plate capacitor that extends into and out of recesses in the semiconductor layer. Maniar is applied to teach a capacitor insulating layer of silicon dioxide or PZT. Maniar is not applied to teach a parallel plate capacitor that extends into and out of recesses in the semiconductor layer. Accordingly, the combination of Vaartstra, Ouellet, and Maniar fails to disclose or suggest a parallel plate capacitor that extends into and out of recesses in the semiconductor layer and claims 21-22 were improperly rejected.

In light of the above, Appellant respectfully requests reversal of the Examiner's rejections of claims 18-22.

Respectfully submitted,

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APPENDIX
CLAIMS ON APPEAL

1-17. (cancelled)

18. (previously presented) An integrated circuit having an analog circuit stage, comprising:

a semiconductor layer having a plurality of recesses formed therein;

a dielectric layer over said semiconductor layer including within said plurality of recesses; and

a parallel plate capacitor over said dielectric layer, said parallel plate capacitor extending into and out of said plurality of recesses in the semiconductor layer.

19. (previously presented) The integrated circuit of claim 18, wherein said parallel plate capacitor comprises a first polysilicon plate.

20. (previously presented) The integrated circuit of claim 19 wherein said parallel plate capacitor comprises a second polysilicon plate.

21. (previously presented) The integrated circuit of claim 18, wherein said parallel plate capacitor comprises a capacitor dielectric of PZT.

22. (previously presented) The integrated circuit of claim 18, wherein said parallel plate capacitor comprises a capacitor dielectric of silicon dioxide.

Evidence Appendix

None.

Related Appeals and Interferences Appendix

None.